



LAYOUT DIAGRAM(原理图): (FIG-1)

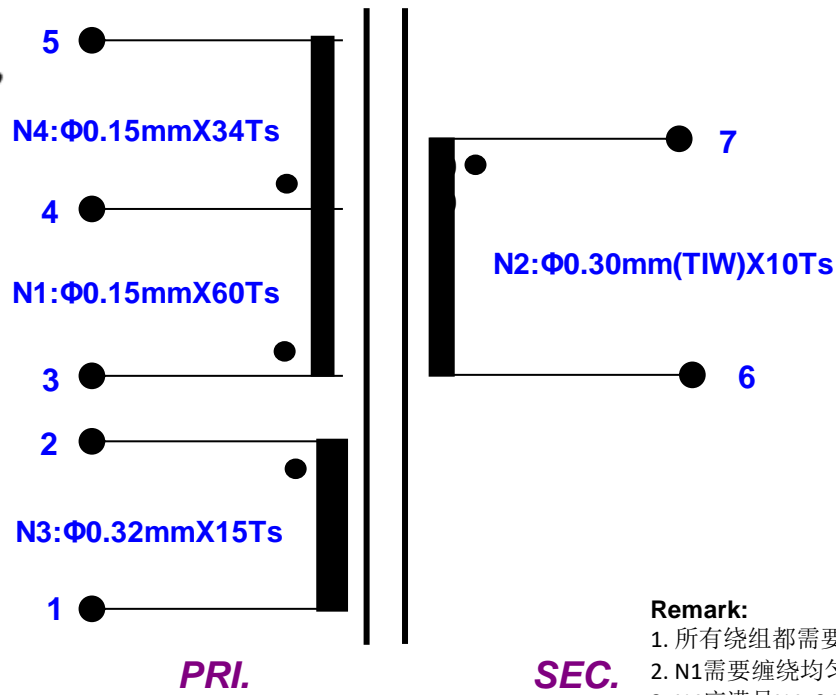


FIG-1

Remark:

1. 所有绕组都需要是平面层，分布均匀。
2. N1需要缠绕均匀紧实，匝数可略少于60圈；
3. N4应满足N4=94-N1的要求，最外层可均匀、轻微缠绕；
4. N2和N3应均匀、轻微缠绕；
5. 引脚8应该被切断。

CROSS SECTION DAGRAM剖视图: (FIG-2)

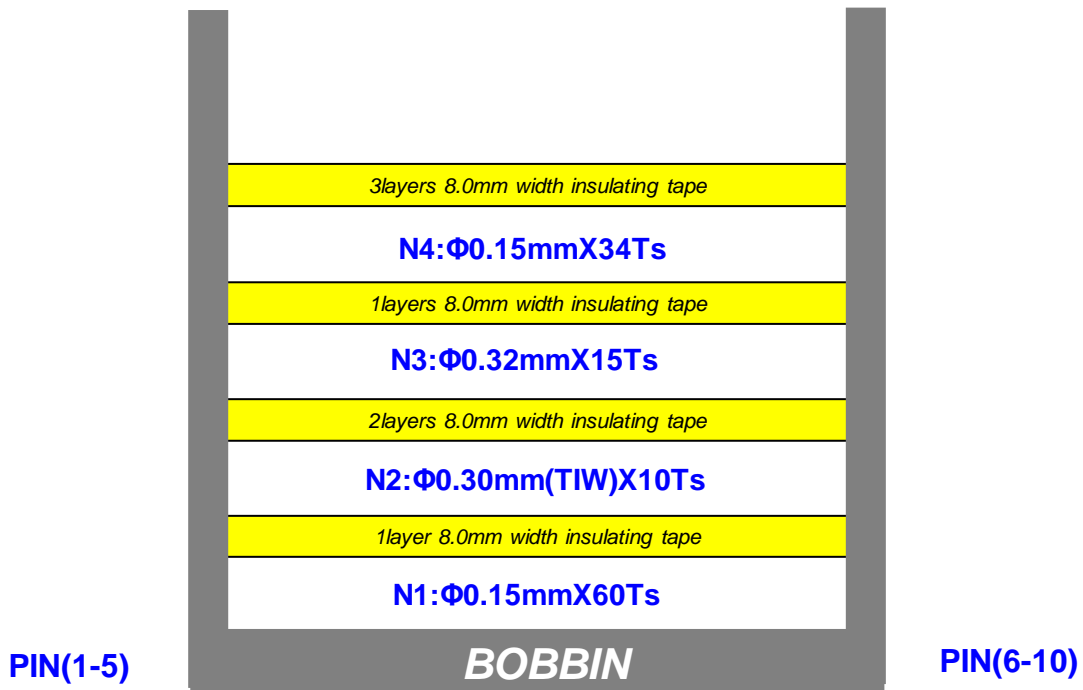


FIG-2

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DATA SPECIFICATION 特性要求: (Table-1)

ITEM 项目	MEASUREMENTS 测试脚位	CHARACTERISTICS 测试范围	MEASURING CONDITIONS 测试条件 (T=25±4°C;HR(%)=45±15)	REMARK 备注
LS 电感	PIN(3-5)	0.91mH±10%	F(kHz)=70 Ug(V)=1	SERIAL MODE 串联模式
LK 漏感	PIN(3-5)	23.0uH MAX	F(kHz)=60 Ug(V)=1 Short Other PINS	SERIAL MODE 串联模式
DCR 直流电阻	PIN(3-5)	3.1Ω MAX	20°C	4 WIRES MODE 四线模式
TURN RATIO 圈数比	PIN(3-5):PIN(7-6):PIN(2-1)	94Ts:10Ts:15Ts±0.5Ts	F(kHz)=20 Ug(V)=1.0	以平面磁芯 测试为准
HIPOT 耐压	PRI./SEC.	NO BREAKDOWN 漏电流≤5.0mA	VAC=3000V/2SEC. F(Hz)=50	/
	PRI./CORE.	NO BREAKDOWN 漏电流≤5.0mA	VAC=500V/2SEC. F(Hz)=50	/
	SEC./CORE.	NO BREAKDOWN 漏电流≤5.0mA	VAC=500V/2SEC. F(Hz)=50	/
	N1./N2.	NO BREAKDOWN 漏电流≤5.0mA	VAC=500V/2SEC. F(Hz)=50	/
COPLANARITY 共平面度	ALL PINS	0.15mm MAX	/	/
PH 相位	REFER TO LAYOUT DIAGRAM FIG-1 参照原理图 FIG-1			

REMARK:初级和次级不相同的两个绕组需测试是否短路

100% testing for the above electrical characteristics.

所有产品按以上要求进行100%测试。

Quality Requirement:(品质要求)

Ref ANSI/ASQC.Z1.4 2008 Level II . Major AQL=0.4% Minor AQL=1.0%.

参照ANSI/ASQC.Z1.4 2008 Level II . Major AQL=0.4% Minor AQL=1.0%.

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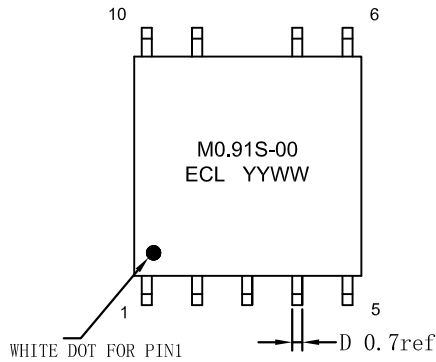


FIG-3

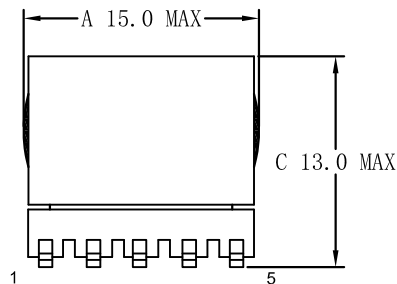


FIG-4

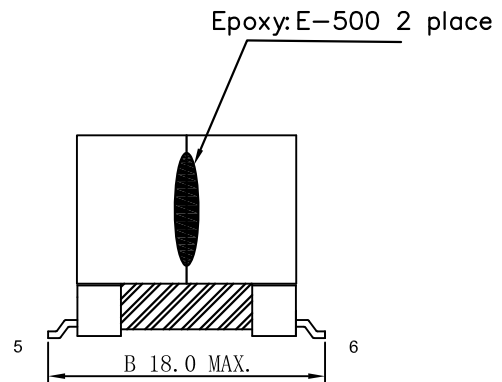


FIG-6

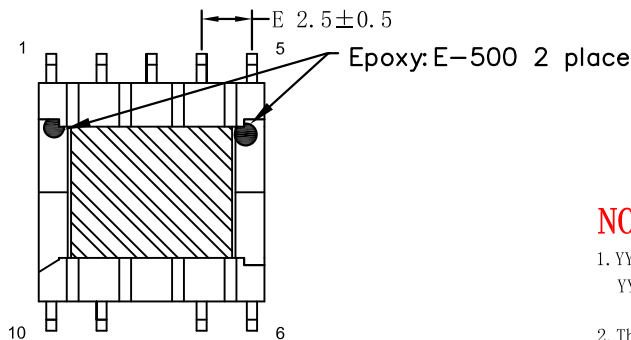


FIG-5

NOTES:

1. YYWW: year week code (FIG-3).
YYWW: 周期年份代码 (FIG-3).
2. The product should be according to RoHS
产品须符合RoHS要求.
3. PIN8 should be cut.
PIN8剪掉

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