

LAYOUT DIAGRAM(原理圖): (FIG-1)

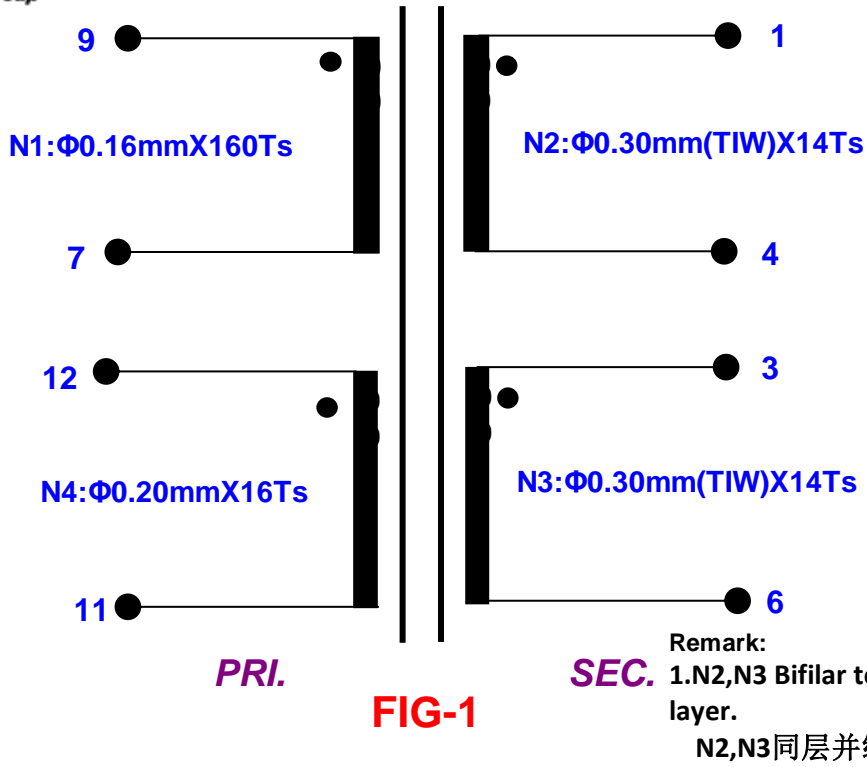


FIG-1

CROSS SECTION DAGRAM剖视图: (FIG-2)

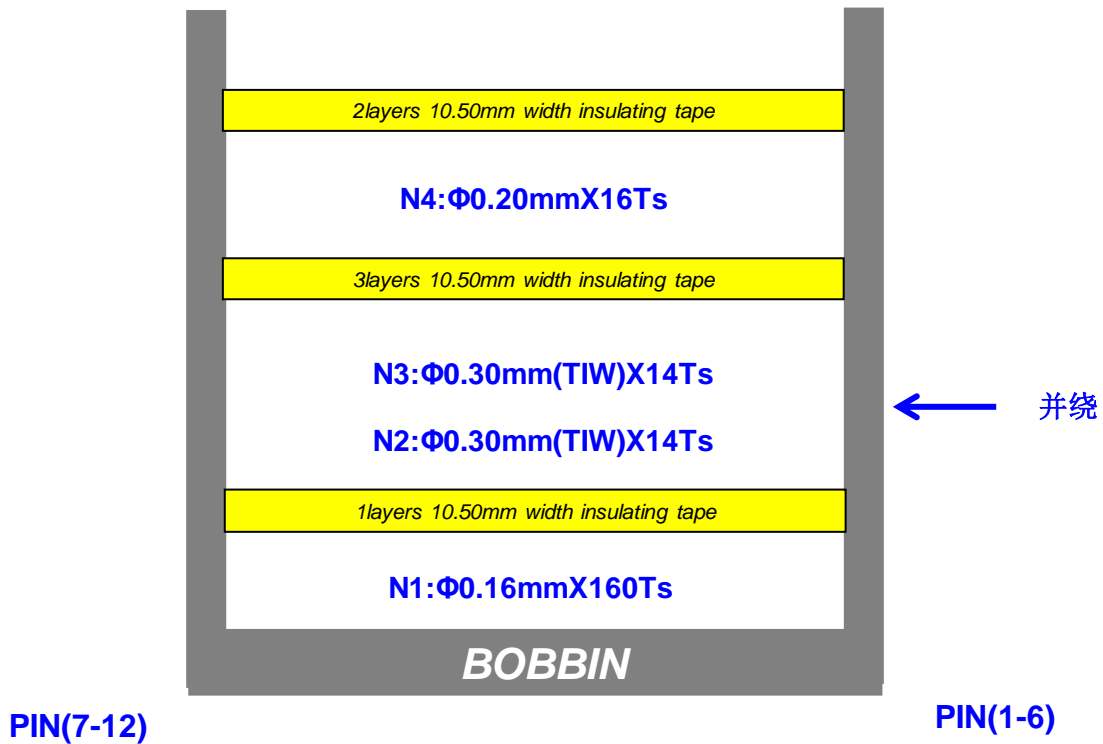


FIG-2

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DATA SPECIFICATION 特性要求: (Table-1)

ITEM 项目	MEASUREMENTS 测试脚位	CHARACTERISTICS 测试范围	MEASURING CONDITIONS 测试条件 (T=20±4℃;HR(%)=45±15)	REMARK 备注
LS 电感	PIN(9-7)	1500uH±10%	F(kHz)=100 Ug(V)=0.1	SERIAL MODE 串联模式
LK 漏感	PIN(9-7)	65uH MAX	F(kHz)=100 Ug(V)=0.1 Short SEC.	SERIAL MODE 串联模式
Rated current max based on inductance change	PIN(9-7)	0.8 A	DC current at which inductance drops 25%(typ) from its value without current	
DCR 直流电阻	PIN(9-7)	4200mΩ MAX	20℃	4 WIRES MODE 四线模式
	PIN(1-4)	140mΩ MAX	20℃	4 WIRES MODE 四线模式
	PIN(3-6)	140mΩ MAX	20℃	4 WIRES MODE 四线模式
	PIN(12-11)	450mΩ MAX	20℃	4 WIRES MODE 四线模式
TURN RATIO 圈数比	N1:N2:N3:N4	160Ts:14Ts:14Ts:16Ts± 0.5Ts	F(kHz)=20 Ug(V)=1.0	以平面磁芯 测试为准
HIPOT 耐压	PRI./SEC.	NO BREAKDOWN 漏电流≤5.0mA	VAC=4000V/2SEC. F(Hz)=50/60	/
	COIL./CORE.	NO BREAKDOWN 漏电流≤5.0mA	VAC=500V/2SEC. F(Hz)=50/60	/
PH 相位	REFER TO LAYOUT DIAGRAM FIG-1 参照原理图 FIG-1			

REMARK:初级和次级不相同的两个绕组需测试是否短路

100% testing for the above electrical characteristics.
所有产品按以上要求进行100%测试.

Quality Requirement:(品质要求)

Ref ANSI/ASQC.Z1.4 2008 Level II . Major AQL=0.4% Minor AQL=1.0%.
参照ANSI/ASQC.Z1.4 2008 Level II . Major AQL=0.4% Minor AQL=1.0%.

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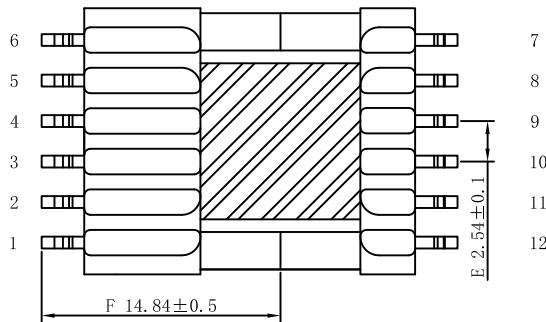


FIG-3

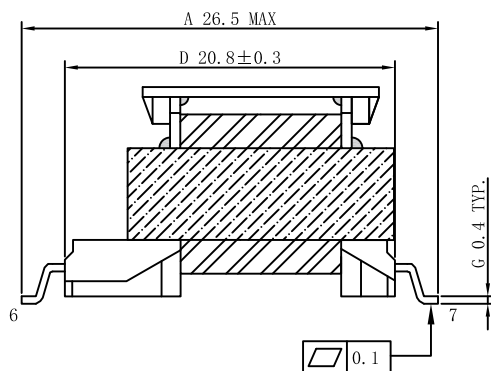


FIG-4

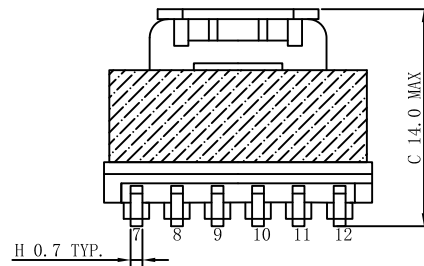


FIG-6

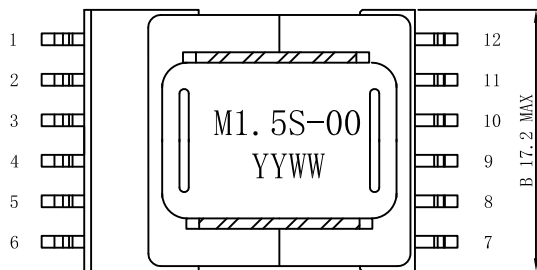


FIG-5

NOTES:

1. Fix two core with 2 layers PF-301 tape.
磁芯缠两圈胶带固定.
2. Fix plastic cap and bobbin and core with epoxy 400-34.
胶帽和骨架以及磁芯用400-34固定.
3. YYWW: year and week code (FIG-5).
YYWW: 年份周期代码 (FIG-5).
4. The part must be complied with RoHS.
产品需满足RoHS要求.

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